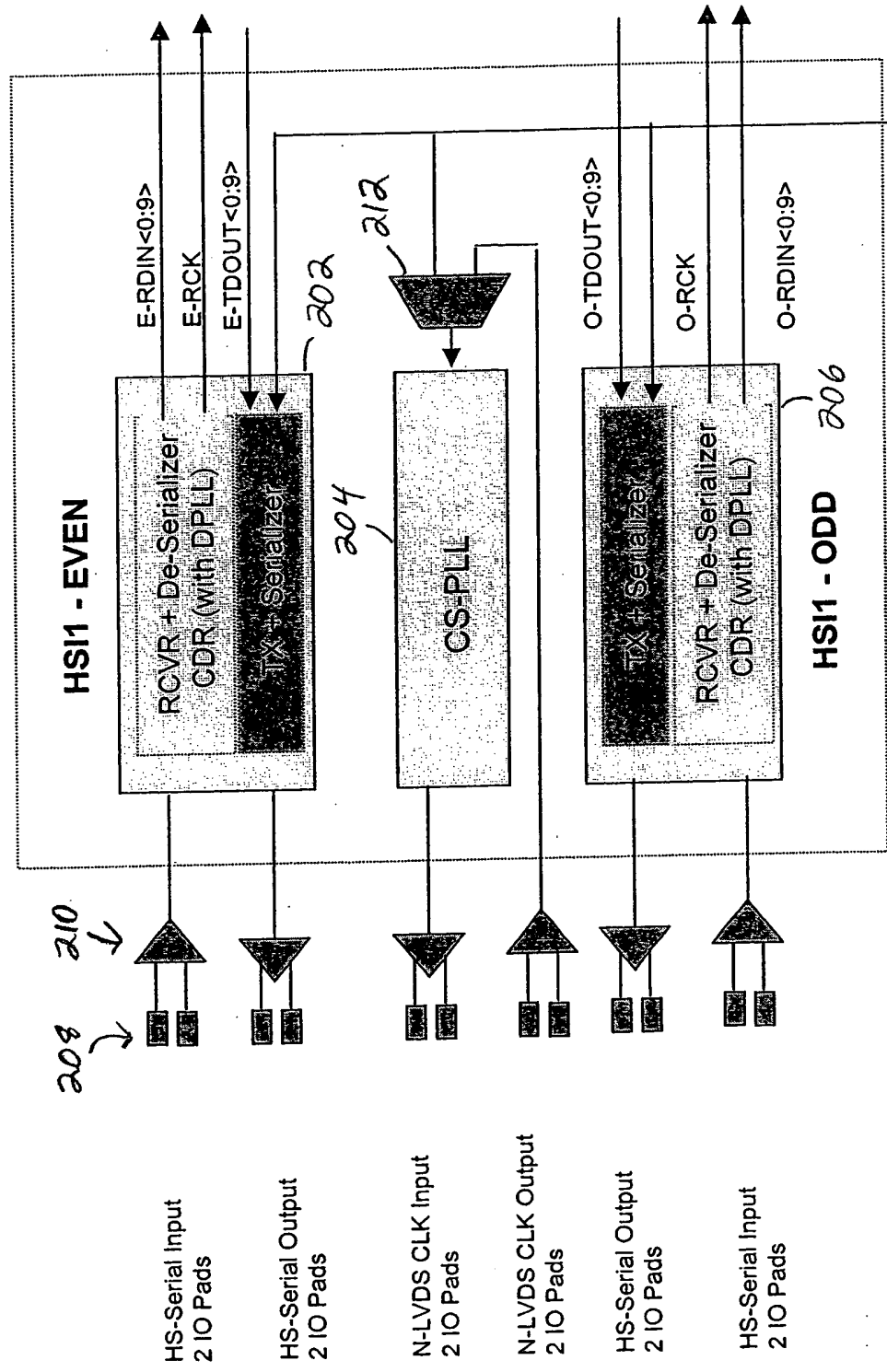


IOs Programmable to be Normal or High Speed Serial IOs

HSI2 Block -- Twin SERDES with CDR & CSPLL



REFCLK <0:3> from Clock Tree

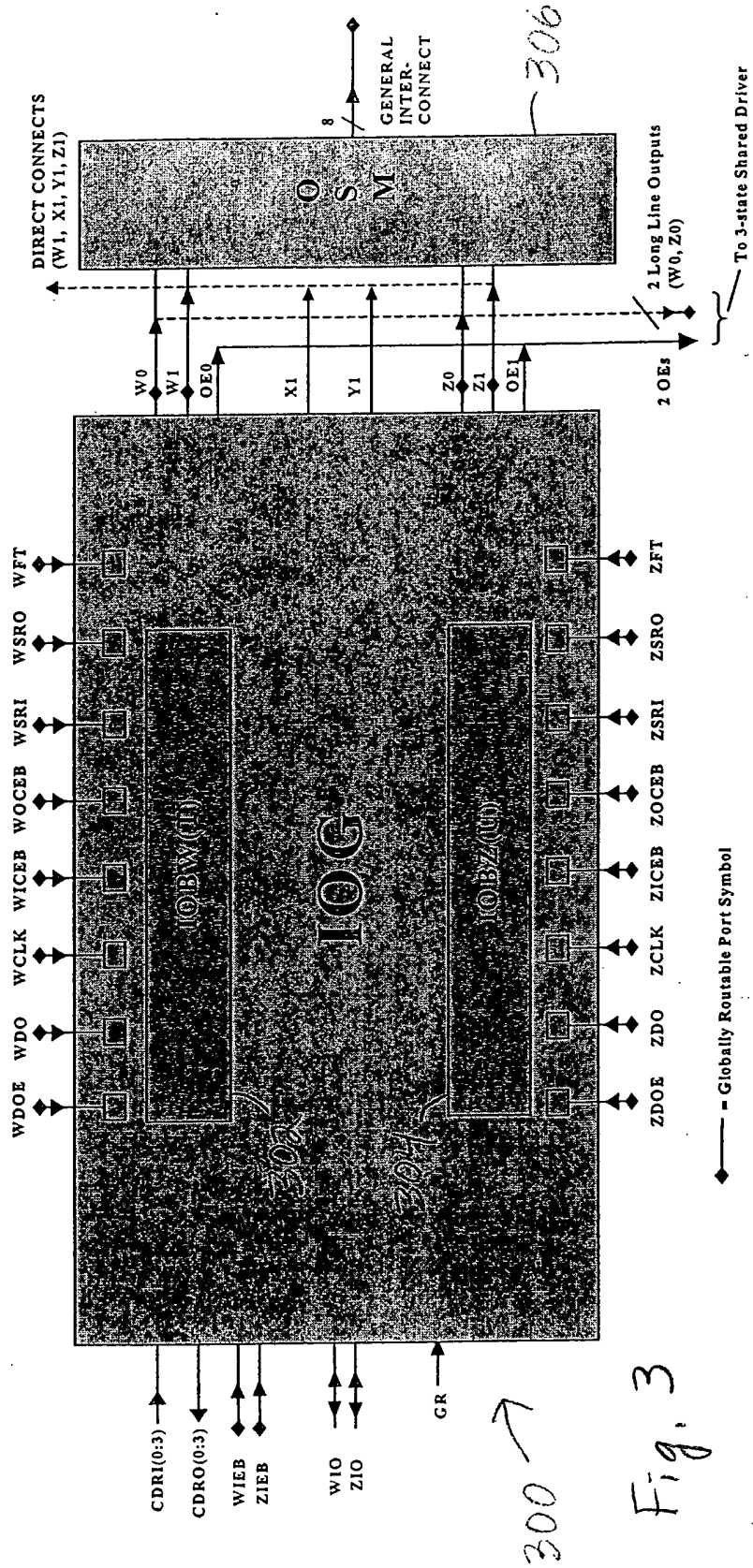
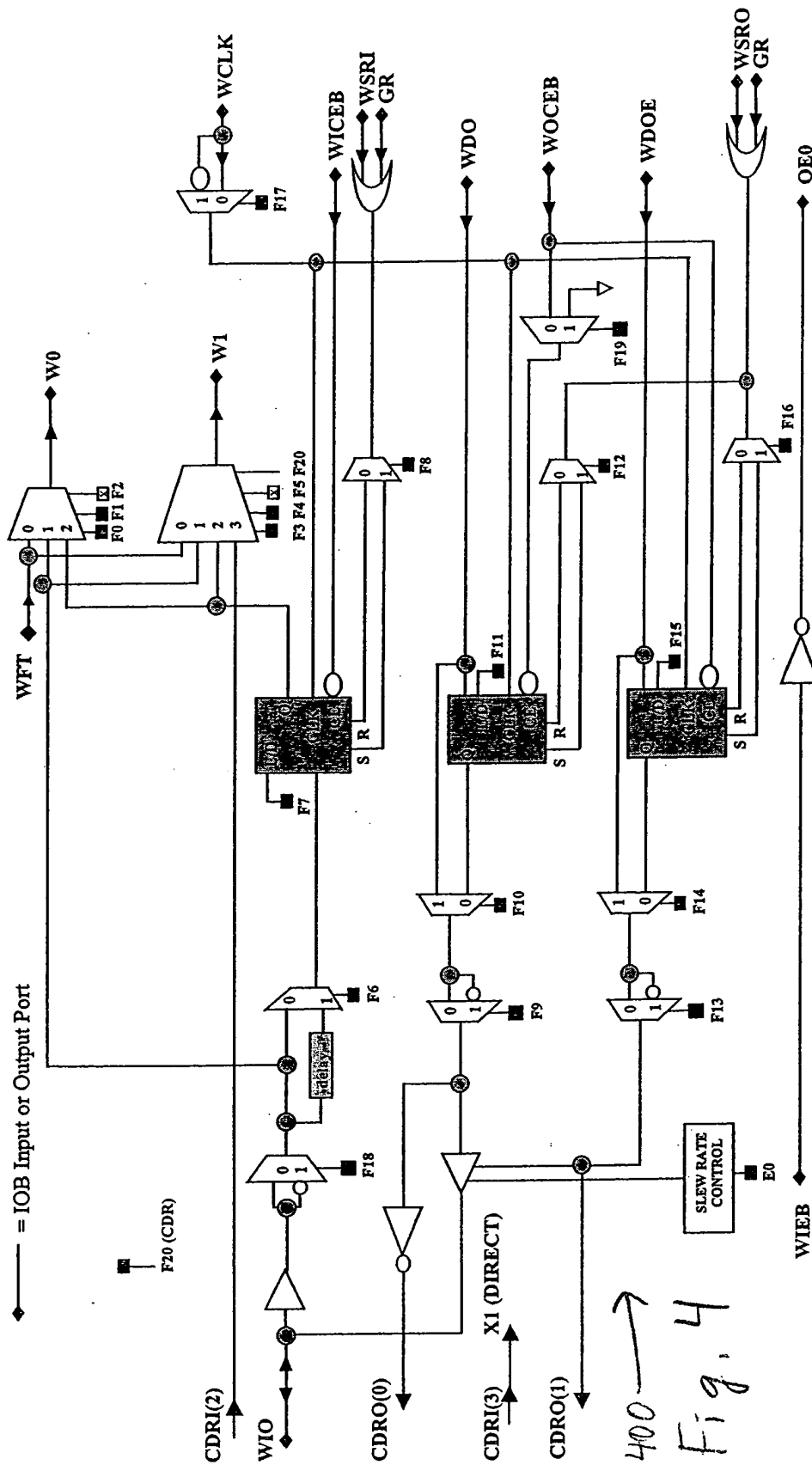
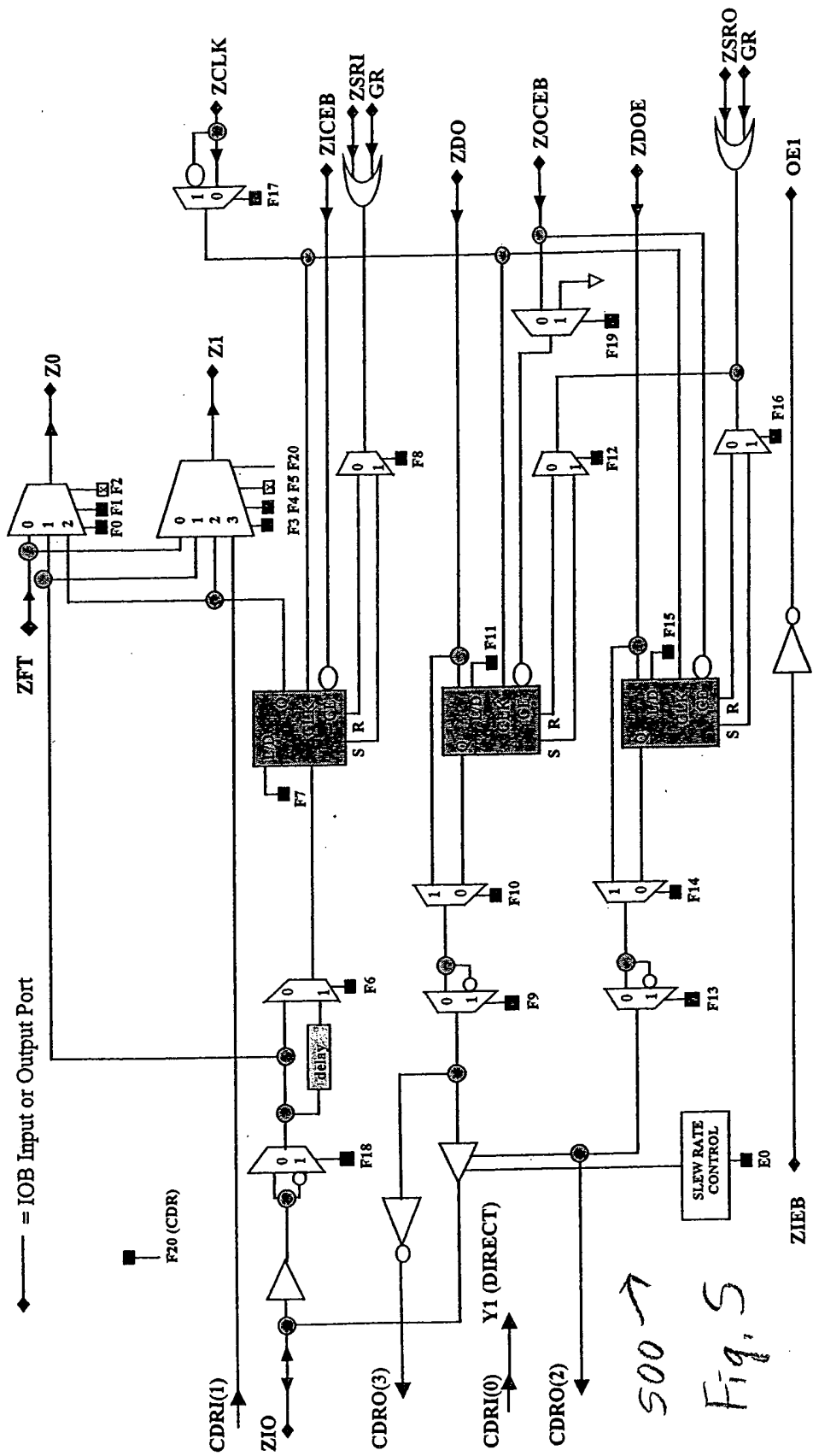


Fig. 3





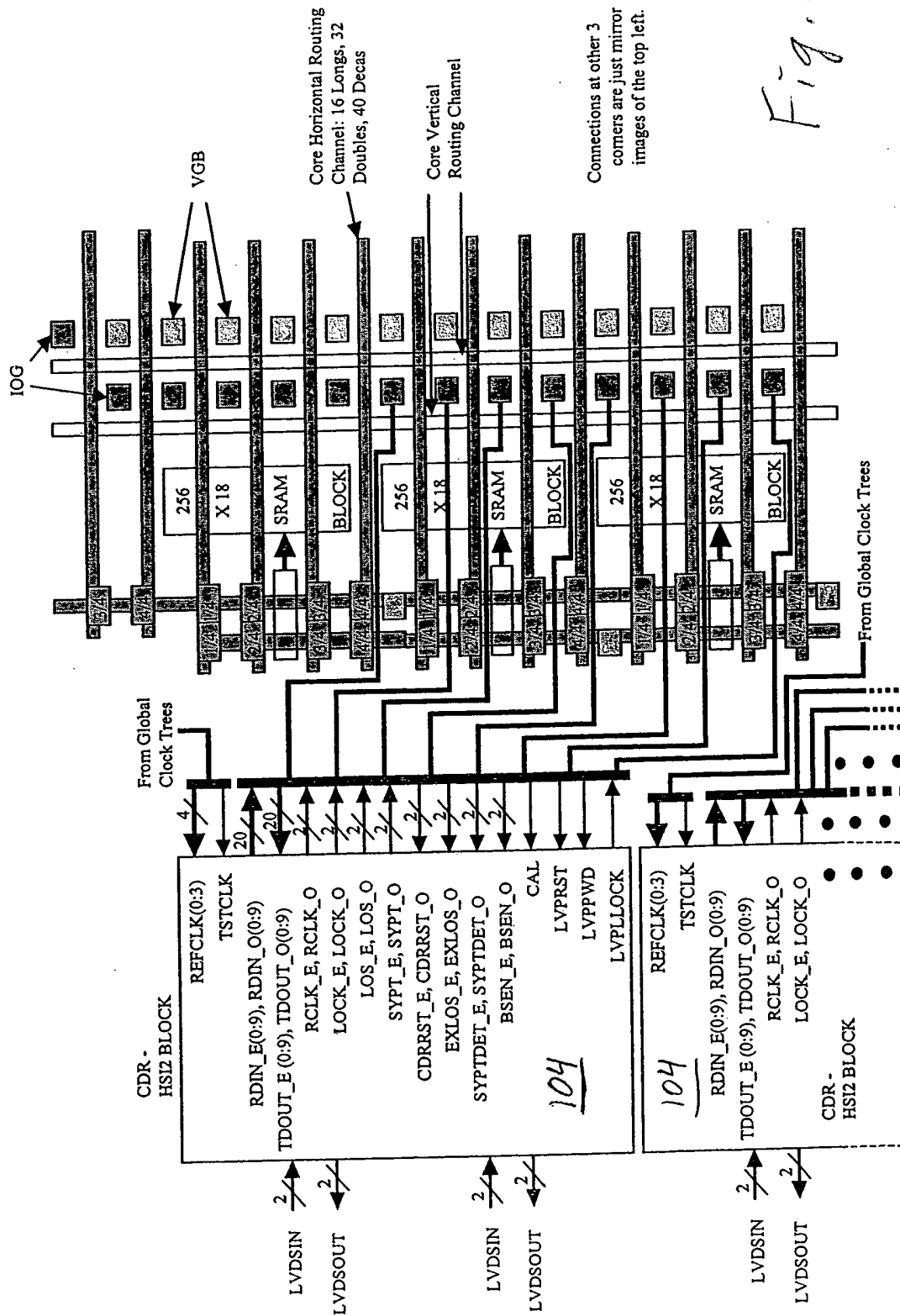


Fig. 6

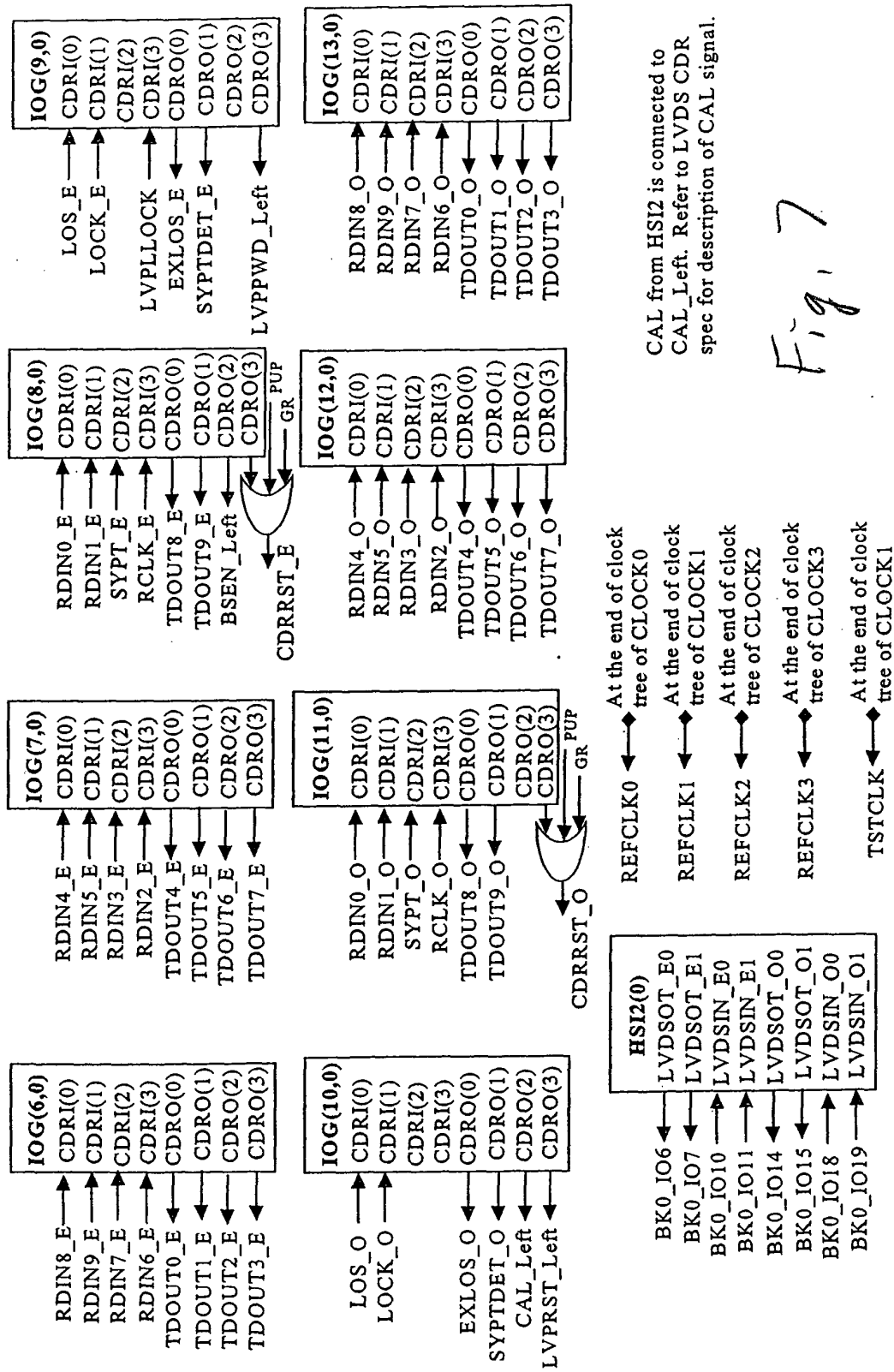


Fig. 7

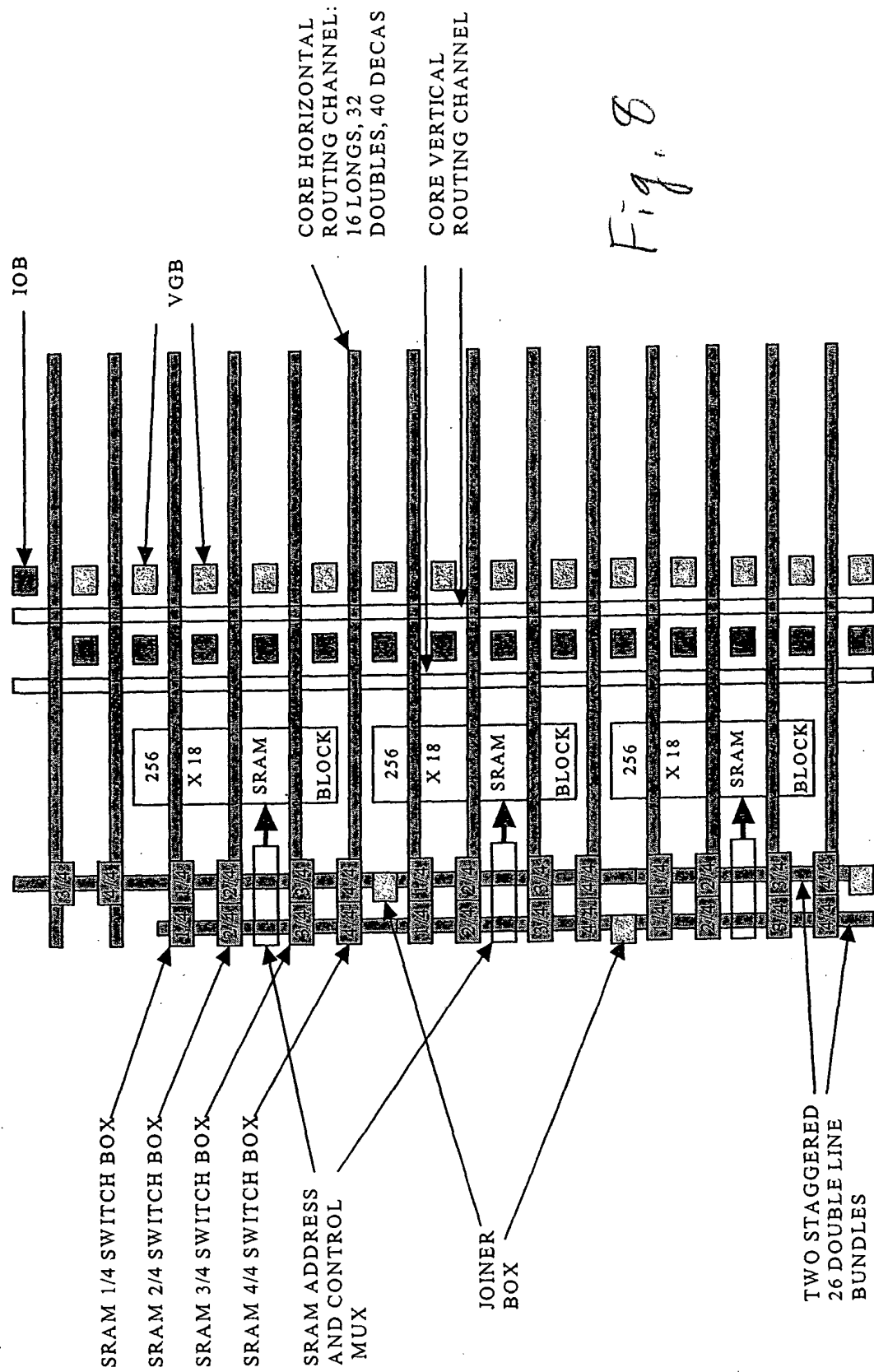


Fig. 8

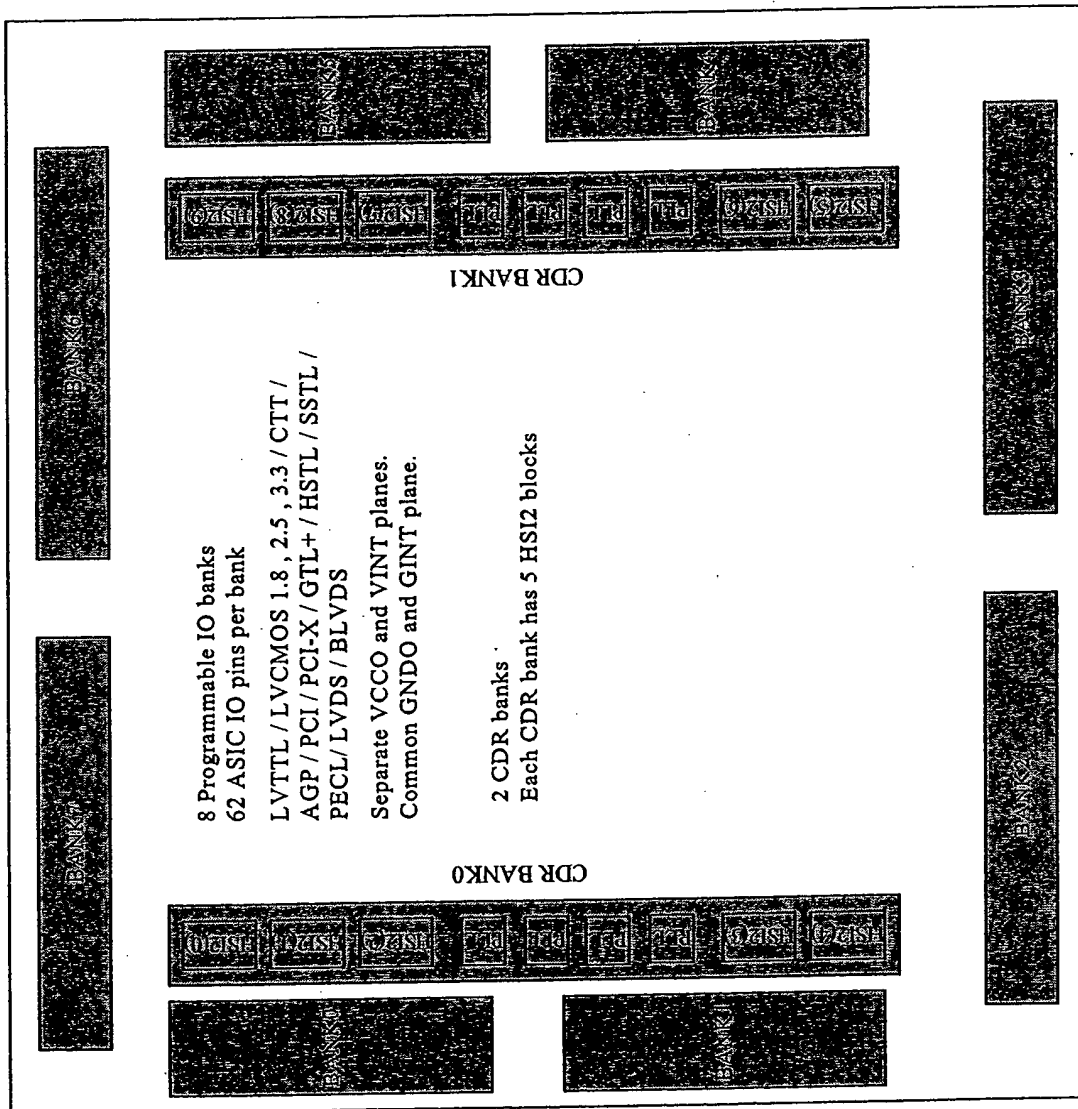


Fig. 9

LAVA1 (X-125 with 2X Memory Blocks, 22x22 GLB Array)

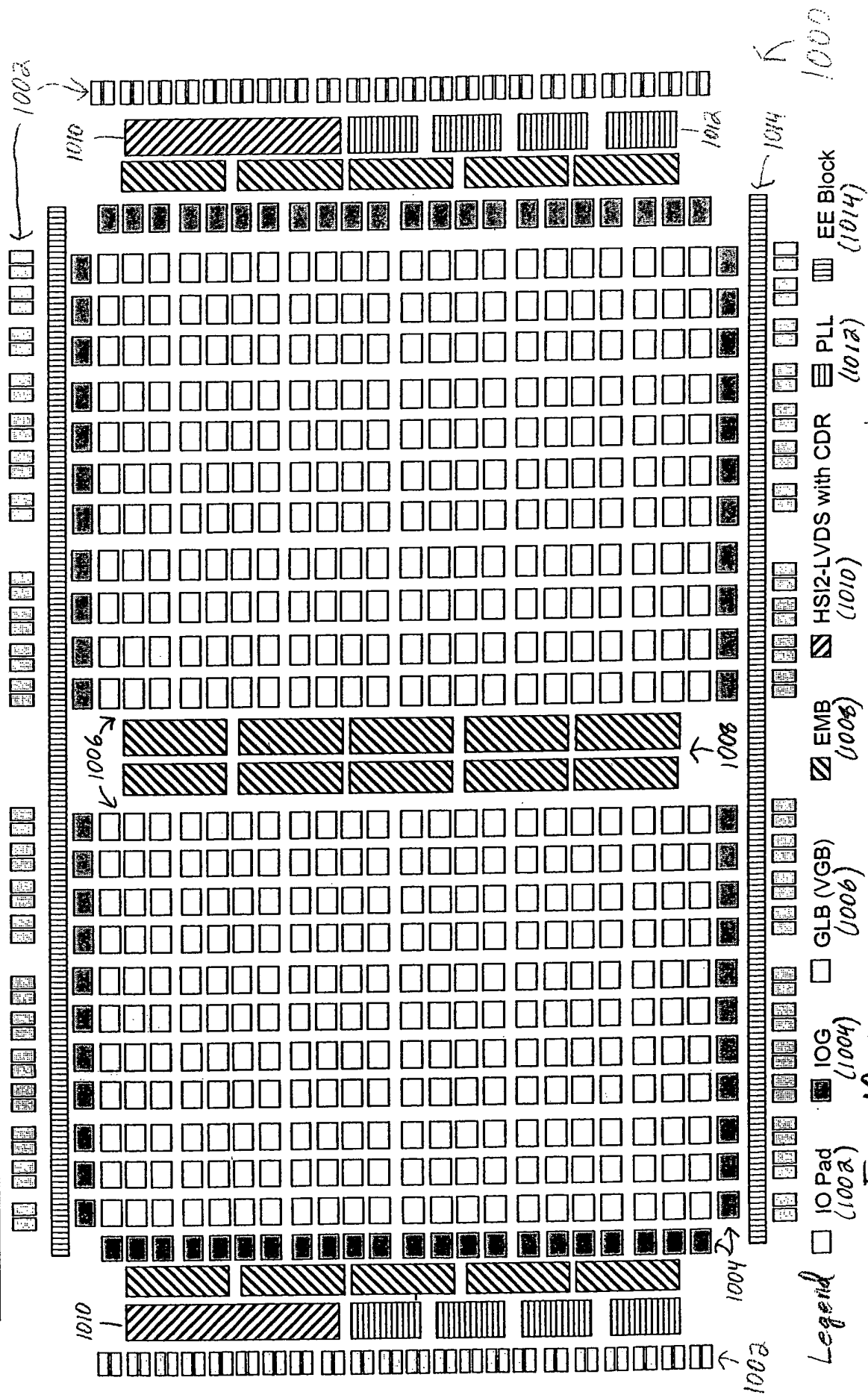
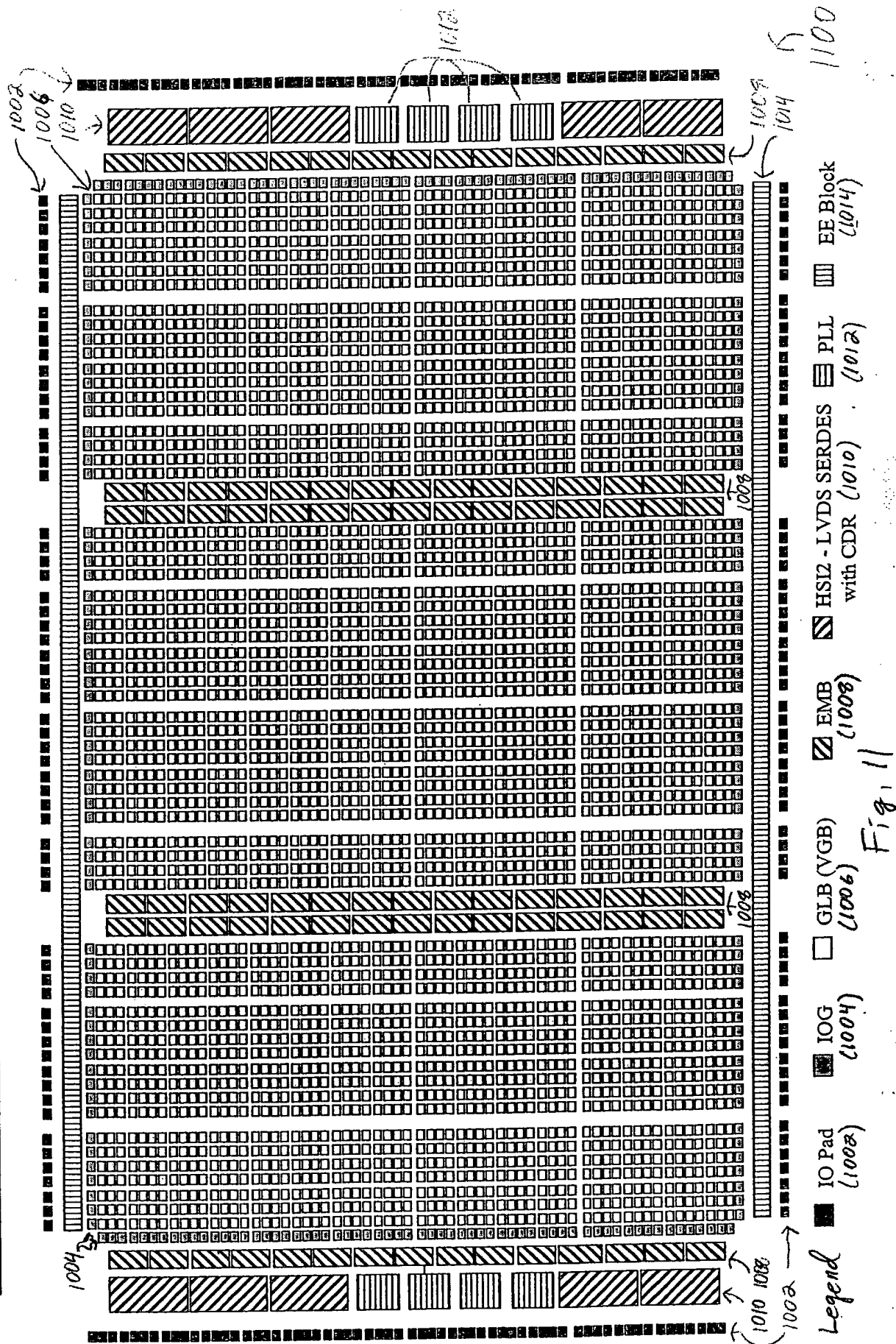
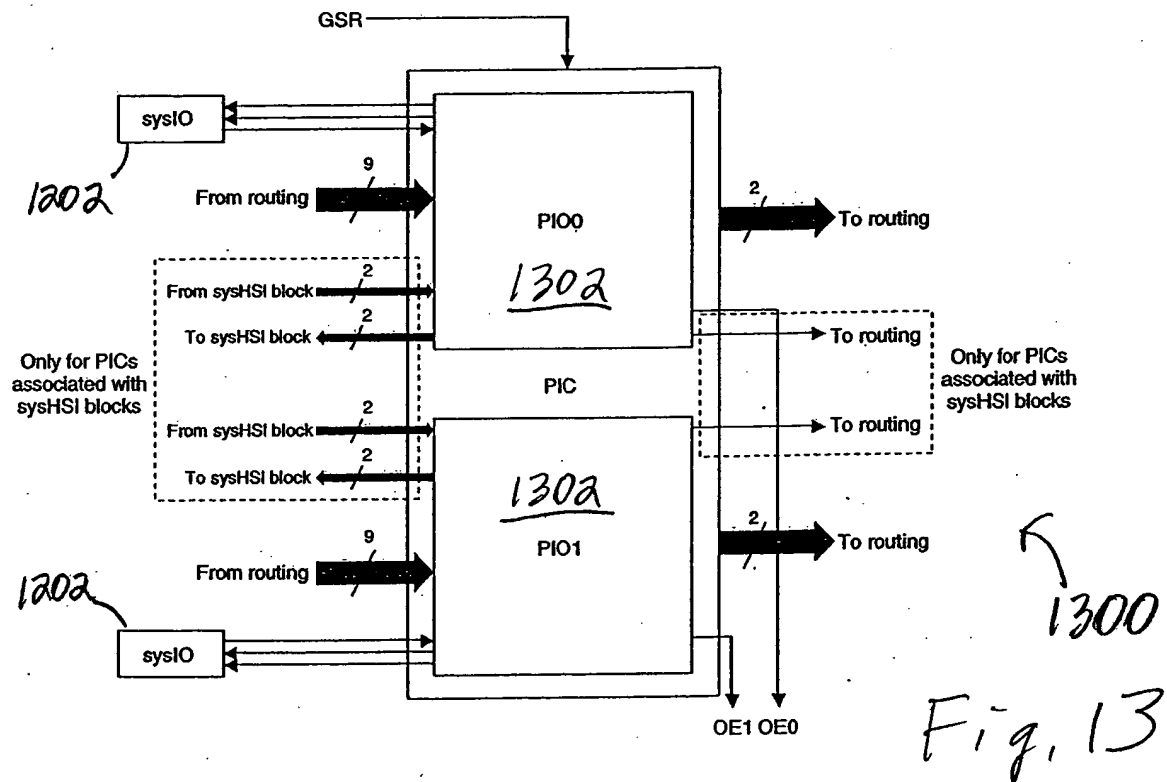
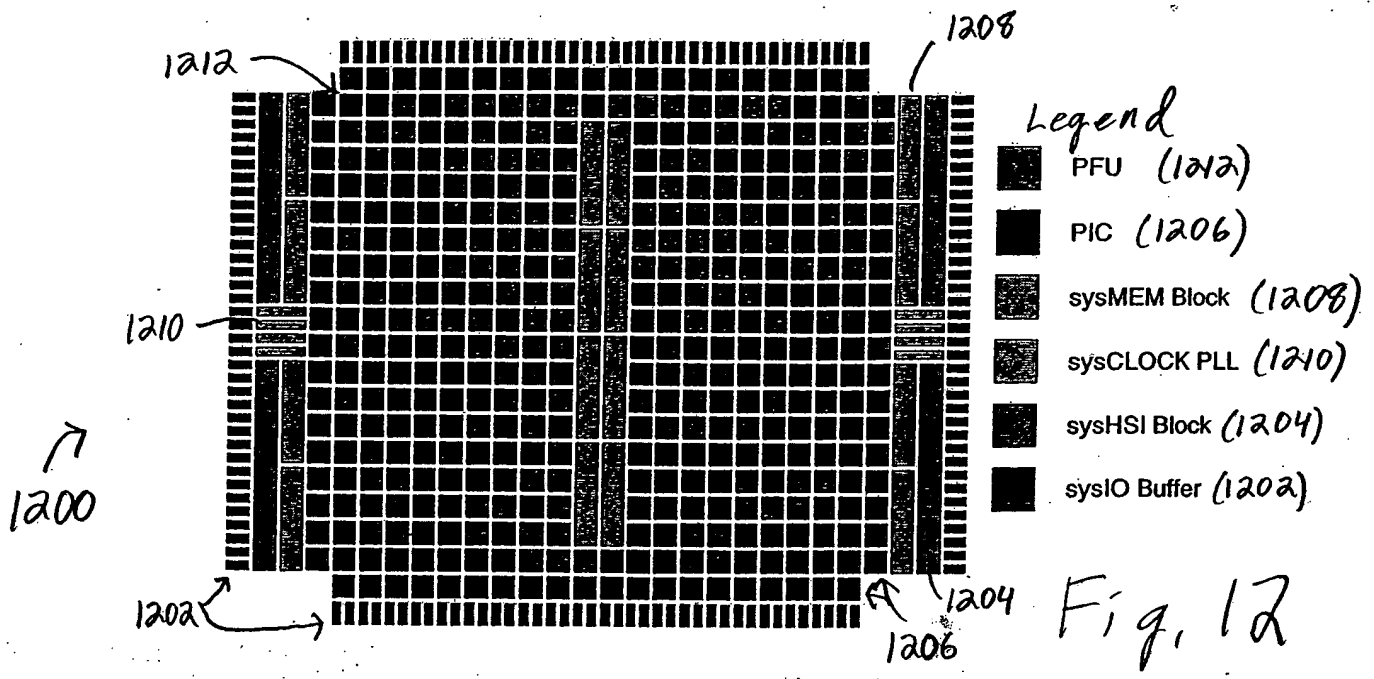


Fig. 10 484 GLBs, 1936 LUTs, 176 IOs, 20 EMBs, 2 HSI2s, 8 PLLs

LAVA1 (X-1200 with 3X Memory Blocks, 62x62 GLB Array)





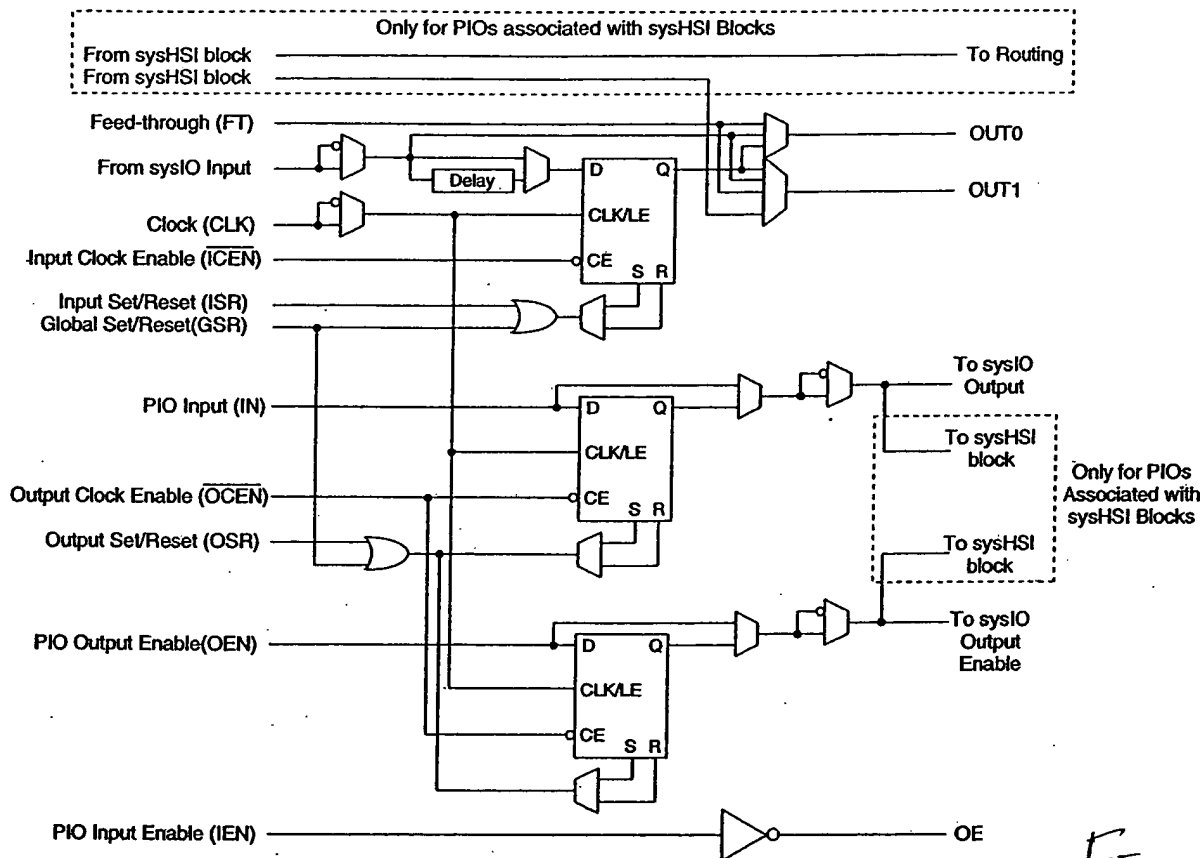


Fig. 14

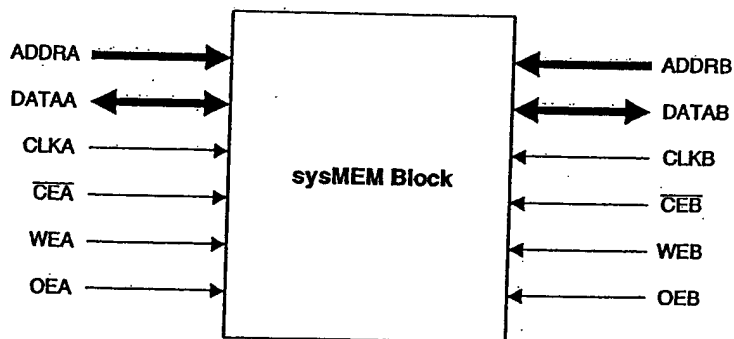


Fig. 15

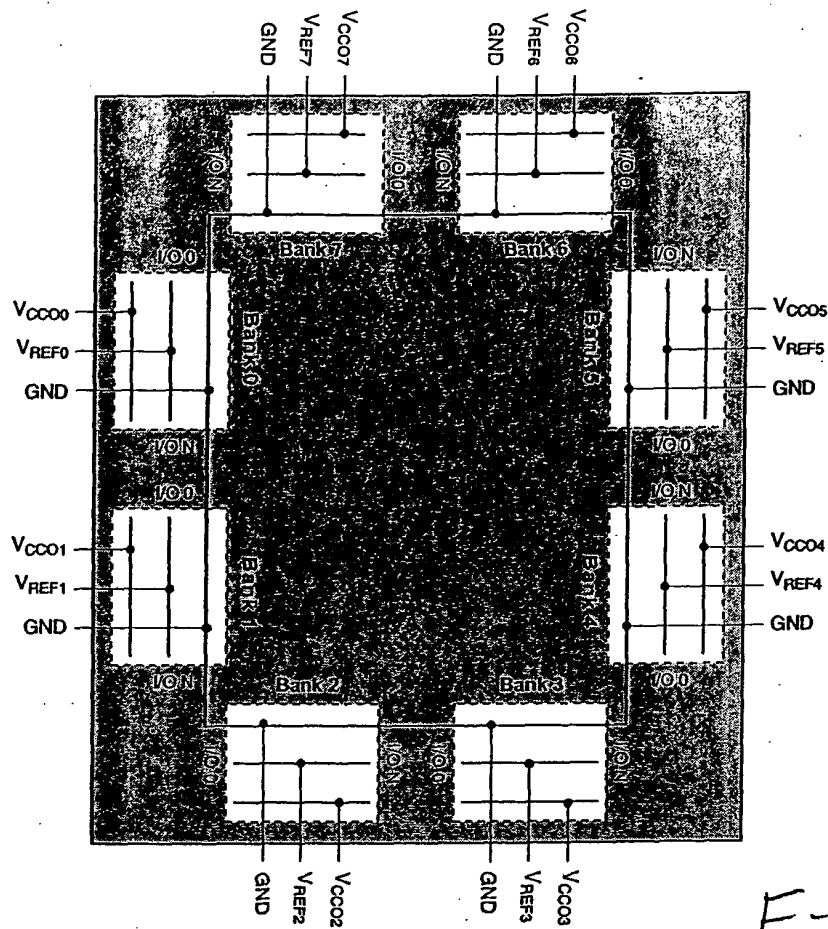


Fig. 16

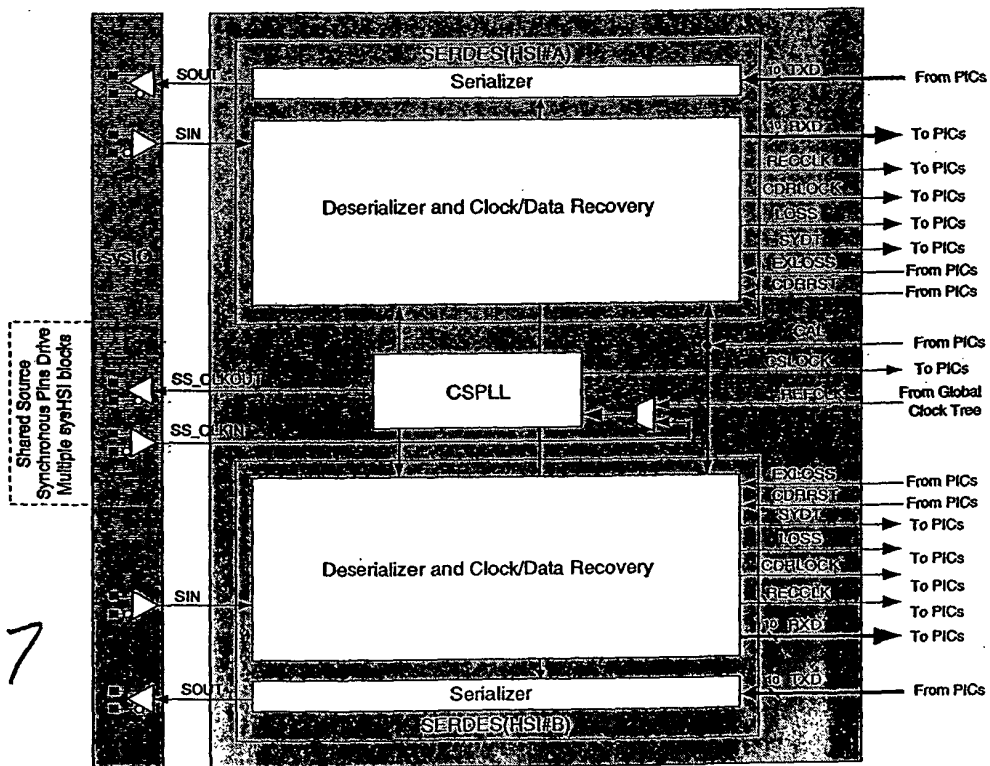


Fig. 17